



Design Automation for Timing-Driven Layout Synthesis (The Springer International Series in Engineering and Computer Science)

S. Sapatnekar, Sung-Mo (Steve) Kang

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Moore's law [Noy77], which predicted that the number of devices integrated on a chip would be doubled every two years, was accurate for a number of years. Only recently has the level of integration begun to slow down somewhat due to the physical limits of integration technology. Advances in silicon technology have allowed designers to integrate more than a few million transistors on a chip; even a whole system of moderate complexity can now be implemented on a single chip. To keep pace with the increasing complexity in very large scale integrated (VLSI) circuits, the productivity of chip designers would have to increase at the same rate as the level of integration. Without such an increase in productivity, the design of complex systems might not be achievable within a reasonable time-frame. The rapidly increasing complexity of VLSI circuits has made design automation an absolute necessity, since the required increase in productivity can only be accomplished with the use of sophisticated design tools. Such tools also enable designers to perform trade-off analyses of different logic implementations and to make well-informed design decisions.

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